SMH Technologies®

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Driver v. 5.01

Moreno Ortolan

Interfacing FlashRunner 2.0 with TDK HVC

SMH Technologies S.r.l.

UNIVERSAL PRODUCTION IN-SYSTEM PROGRAMMING

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TDK HVC Introduction

HVC with Arm Cortex-M3 MCUs

The HVC 4x flex servo-drive family from TDK-Micronas enables cost-effective realization of high-performance compact electric motor control.

The new HVC 4422F offers extended memory size to address the OEM diagnostic requirements and allows operation in high-temperature environments. An integrated MPU supports RTOS requirements.

Powered by a 32-bit CPU core (Arm® Cortex®-M3), the HVC controllers economically address growing challenges in the automotive market and beyond (industrial, consumer, instrumentation, etc.).
The flexible peripherals of the product provide all means to directly control brush-type, stepper (bipolar or three phase), or brushless (BLDC) motors directly via the integrated high-performance half-bridges without the need for external driver components.

Beside timers/counters, interrupt controller, multichannel ADC, SPI, and enhanced PWMs with diagnostic functions, these devices contain an advanced LIN UART with a LIN 2.x transceiver, as well as voltage regulators to connect the device directly to an automotive board net. Various power management modes optimize current consumption.

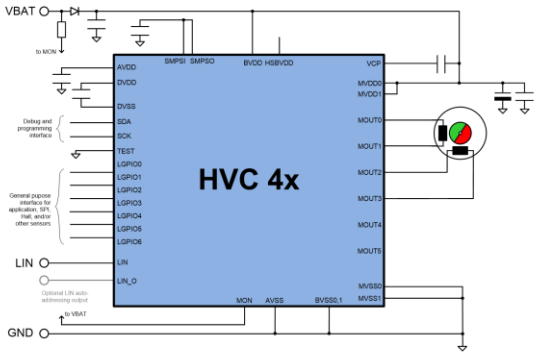
The HVC family further features a flash program memory with a size of 32 KBytes (HVC 4222/4223) or 64 KBytes (HVC 4420F/4422), providing high flexibility in code development, production ramp-up, and in-system firmware update.

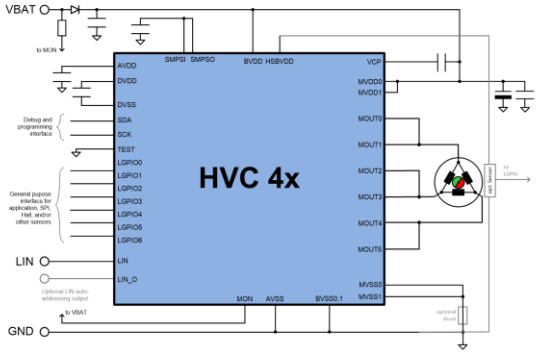
Various integrated digital and analog circuit units such as comparators with virtual star point reference, current scaling and an embedded programmable gain amplifier allow users to minimize the number of external components.

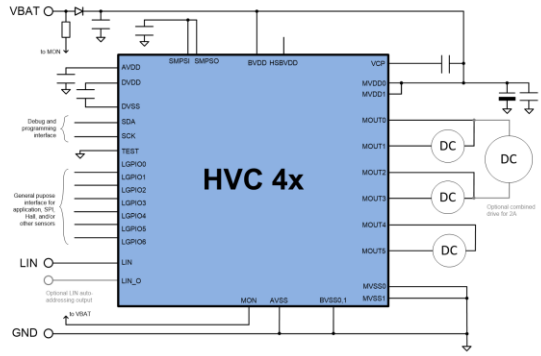
The computation capacity supports complex motor control algorithms such as Space Vector Modulation (SVM) for Permanent-Magnet Synchronous Motors (PMSM) in addition to six-step commutation with sensor feedback or sensorless control, as well as various stepper configurations.

HVC Variants:

HVC 4222F - 32k Flash - 2k RAM - T_A = 150 °C
HVC 4223F - 32k Flash - 2k RAM - T_A = 125 °C
HVC 4420F - 64k Flash - 4k RAM - T_A = 125 °C
HVC 4422F - 64k Flash - 4k RAM - T_A = 150 °C







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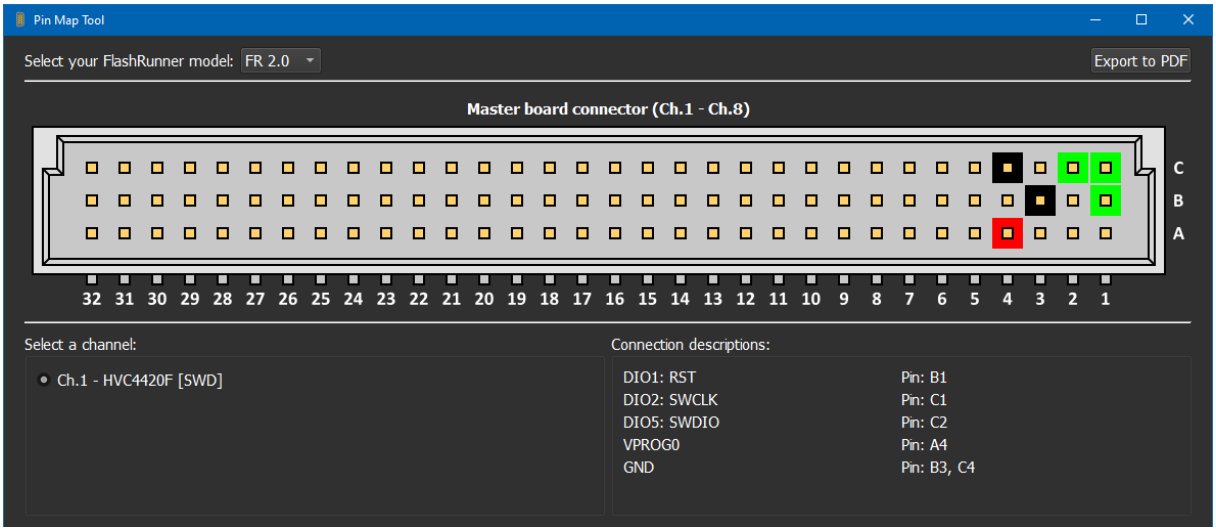
TDK HVC Protocol and PIN map

HVC devices support the SWD protocol.

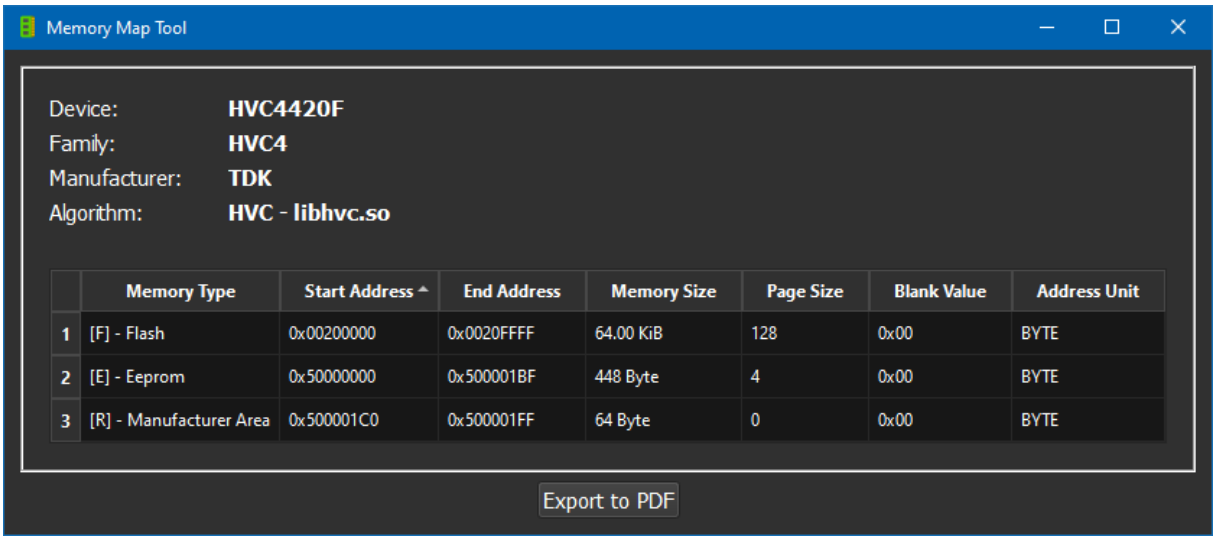
```
#TCSETPAR CMODE <SWD>
```

TDK HVC PIN MAP



TDK HVC Memory Map

Memory Type	Start Address	End Address	Memory Size	Page Size	Blank Value	Address Unit
[F] – Flash	0x00200000	0x0020FFFF	64.00 KiB	128	0x00	BYTE
[E] – Eeprom	0x50000000	0x50C001BF	448 Byte	4	0x00	BYTE
[R] – Manufacturer Area	0x500001C0	0x500001FF	64 Byte	0	0x00	BYTE



	Memory Type	Start Address	End Address	Memory Size	Page Size	Blank Value	Address Unit
1	[F] - Flash	0x00200000	0x0020FFFF	64.00 KiB	128	0x00	BYTE
2	[E] - Eeprom	0x50000000	0x500001BF	448 Byte	4	0x00	BYTE
3	[R] - Manufacturer Area	0x500001C0	0x500001FF	64 Byte	0	0x00	BYTE

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TDK HVC Driver Parameters

The standard parameters are used to configure some specific options inside HVC driver.

#TCSETPAR ENTRY_CLOCK

Syntax: `#TCSETPAR ENTRY_CLOCK <Frequency>`

`<Frequency>` Accepted parameters 4000000, 2000000, 1000000, 500000, 100000 Hz

Description: Set the SWD frequency used in the Connect procedure before raising the PLL of the device, if the device PLL is available

Note: Default value 4.00 MHz

#TCSETPAR SAMPLING_POINT

Syntax: `#TCSETPAR SAMPLING_POINT <Value>`

`<Value>` Accepted values are in the range 1-15

Description: Use this parameter to permanently set the sampling point of the FPGA
It is recommended to leave this parameter with the default value

Note: Default value 17

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TDK HVC Driver Commands

Here you can find the complete list of all available commands for HVC driver.

```
Memory type:

F → Flash
E → Eprom
R → Manufacturer Area (Reserved)
```

#TPCMD CONNECT

#TPCMD CONNECT

This function performs the entry and is the first command to be executed when starting the communication with the device.

```
---#TPCMD CONNECT
Protocol selected SWD.
Entry Clock is 1.00 MHz.
Trying Hot Plug connect procedure.
IDCODE: 0x2BA01477.
Designer: 0x23B, Part Number: 0xBA01, Version: 0x2.
ID-Code read correctly at 1.00 MHz.
JTAG-SWD Debug Port enabled.
Scanning AP map to find all APs.
AP[0] IDR: 0x24770011, Type: AMBA AHB3 bus.
AP[0] ROM table base address 0xE00FF000.
CPUID: 0x412FC231.
Implementer Code: 0x41 - [ARM].
Found Cortex M3 revision r2p1.
Cortex M3 Core halted [0.001 s].
Device chip version:
 * Device official code is HVC4420.
 * Device version is B1.
 * Device CUST is 0xF (Flash).
 * Device ROM version 0x0 (Flash).
 * SWD Debug Interface is enabled.
 * Window Watchdog is not enabled.
 * Digital Watchdog is not enabled.
Requested Clock is 37.50 MHz.
Generated Clock is 37.50 MHz.
Good samples: 3 [Range 4-6].
IDCODE: 0x2BA01477.
Designer: 0x23B, Part Number: 0xBA01, Version: 0x2.
ID-Code read correctly at 37.50 MHz.
Time for Connect: 0.107 s.
>|
```

When the device is Readout Protected you can see the following entry:

```
---#TPCMD CONNECT
Protocol selected SWD.
Entry Clock is 4.00 MHz.
Trying Hot Plug connect procedure.
IDCODE: 0x2BA01477.
Designer: 0x23B, Part Number: 0xBA01, Version: 0x2.
ID-Code read correctly at 4.00 MHz.
JTAG-SWD Debug Port enabled.
Scanning AP map to find all APs.
AP[0] IDR: 0x24770011, Type: AMBA AHB3 bus.
AP[0] ROM table base address 0xE00FF000.
Could not establish a complete connection to target:
 * Unable to read the Cortex CPUID register.
 * Probably the HVC device is Readout Protected.
0800018F!|
01|ERR--08000100|[file ../Code/HVC_2_ALGO.c, line 256, funct SWDentry()]
01|ERR--08000100|[file ../Code/HVC_2_ALGO.c, line 69, funct ProgrammingEntry()]
01|ERR--0800018F|[file ../Code/HVC_1_API.c, line 399, funct CmdConnect()]
01|ERR--0800018F|[file ../Src/pi-algo.c, line 687, funct cmd_TPCMD()]
```


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#TPCMD MASSERASE

```
#TPCMD MASSERASE <F>
```
Use this command to erase the entire Flash memory.

#TPCMD ERASE

```
#TPCMD ERASE <F>
#TPCMD ERASE <F> <start address> <size>
```
With this command, a Sector Erase of the Flash memory will be performed.
Typically running the Sector Erase command takes much longer than running the Masserase command.
Enter the Start Address and Size in hexadecimal format.

#TPCMD BLANKCHECK

```
#TPCMD BLANKCHECK <F>
#TPCMD BLANKCHECK <F> <start address> <size>
```
Verify if selected part of the Flash memory is erased.
Enter the Start Address and Size in hexadecimal format.

#TPCMD PROGRAM

```
#TPCMD PROGRAM <F|E>
#TPCMD PROGRAM <F|E> <start address> <size>
```
Program selected part of Flash or Eeprom memory.
Enter the Start Address and Size in hexadecimal format.

#TPCMD VERIFY

```
#TPCMD VERIFY <F|E> <R>
#TPCMD VERIFY <F|E> <R> <start address> <size>
```
R: Readout Mode.
Verify selected part of Flash or Eeprom memory through Readout method.
Enter the Start Address and Size in hexadecimal format.

```
#TPCMD VERIFY <F> <S>
#TPCMD VERIFY <F> <S> <start address> <size>
```
S: Checksum 32 Bit Mode.
Verify selected part of Flash through Checksum 32Bit method.
Enter the Start Address and Size in hexadecimal format.

#TPCMD READ

```
#TPCMD READ <F|E|R>
#TPCMD READ <F|E|R> <start address> <size>
```
Read selected part of Flash, Eeprom or Manufacturer Area memory.
The result of the read command will be visible into the Terminal.
Enter the Start Address and Size in hexadecimal format.

#TPCMD DUMP

```
#TPCMD DUMP <F|E|R>
#TPCMD DUMP <F|E|R> <start address> <size>
```
Dump selected part of Flash, Eeprom or Manufacturer Area memory.
The result of the dump command will be stored in the FlashRunner 2.0 internal memory.
Enter the Start Address and Size in hexadecimal format.

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#TPCMD SET_READOUT_PROTECTION

Syntax: `#TPCMD SET_READOUT_PROTECTION`

Prerequisites: none

Description: Set the Readout Protection into target HVC device
This command set to 0 the NVRAM_CONFIG.DBGEN bit into NVRAM memory
This protection is not reversible from the debugger
The debug interface can be re-enabled again by setting NVRAM_CONFIG.DBGEN = 1 only if the application software inside the HVC device provides a corresponding code sequence and an interface to trigger it

Note: This command is available from **libhvc.so** version **5.01**

Examples: Correct command execution: 😊

```
---#TPCMD SET_READOUT_PROTECTION
Enabling HVC Readout Protection.
Time for Set Readout Protection: 0.003 s.
```

#TPCMD READ_MEM8

Syntax: `#TPCMD READ_MEM8 <Address> <Byte Count>`

<Address>	Address in HEX format (i.e., 0x52002020)
<Byte Count>	Byte count in decimal format (i.e., 8 -> eight bytes)

Prerequisites: none

Description: Read memory byte per byte from target HVC device

Note: This command prints into Terminal and Real Time Log

Examples: Correct command execution: 😊

```
---#TPCMD READ_MEM8 0x52002020 8
Read[0x52002020]: 0xF0
Read[0x52002021]: 0xAA
Read[0x52002022]: 0x16
Read[0x52002023]: 0x14
Read[0x52002024]: 0x00
Read[0x52002025]: 0x00
Read[0x52002026]: 0x00
Read[0x52002027]: 0x00
Time for Read Mem: 0.002 s
```

#TPCMD READ_MEM16

Syntax: `#TPCMD READ_MEM16 <Address> <16-bit Word Count>`

<Address>	Address in HEX format (i.e., 0x52002020)
<16-bit Word Count>	16-bit Word count in decimal format (i.e., 4 -> four 16-bit words)

Prerequisites: none

Description: Read memory 16-bit word per 16-bit word from target HVC device

Note: This command prints into Terminal and Real Time Log

Examples: Correct command execution: 😊

```
---#TPCMD READ_MEM16 0x52002020 4
Read[0x52002020]: 0xAAF0
Read[0x52002022]: 0x1416
```


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```
Read[0x52002024]: 0x0000
Read[0x52002026]: 0x0000
Time for Read Mem: 0.002 s
```

#TPCMD READ_MEM32

Syntax: `#TPCMD READ_MEM32 <Address> <32-bit Word Count>`

<Address>	Address in HEX format (i.e., 0x52002020)
<32-bit Word Count>	32-bit Word count in decimal format (i.e., 2 -> two 32-bit words)

Prerequisites: none

Description: Read memory 32-bit word per 32-bit word from target HVC device

Note: This command prints into Terminal and Real Time Log

Examples: Correct command execution: 😊

```
---#TPCMD READ_MEM32 0x52002020 2
Read[0x52002020]: 0x1416AAF0
Read[0x52002024]: 0x00000000
Time for Read Mem: 0.002 s
```

#TPCMD DISCONNECT

`#TPCMD DISCONNECT`

Disconnect function. Power off and exit.

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TDK HVC Driver Examples

Here you can see a complete example of TDK HVC projects.

1 – TDK HVC 64KB example Commands

HVC4420F

```
#TCSETPAR ENTRY_CLOCK 4000000
#TCSETPAR PROTCLK 37500000
#TCSETPAR PWDOWN 100
#TCSETPAR PWUP 100
#TCSETPAR RSTDOWN 100
#TCSETPAR RSTDRV OPENDRAIN
#TCSETPAR RSTUP 100
#TCSETPAR VPROG0 3300
#TCSETPAR CMODE SWD
#TPSETSRC 64KB.frb
#TPSTART
#TPCMD CONNECT
#TPCMD MASSERASE F
#TPCMD BLANKCHECK F
#TPCMD PROGRAM F
#TPCMD VERIFY F R
#TPCMD VERIFY F S
#TPCMD DISCONNECT
#TPEND
```

1 – TDK HVC 64KB example Real Time Log

```
---#TPCMD CONNECT
Protocol selected SWD.
Entry Clock is 1.00 MHz.
Trying Hot Plug connect procedure.
IDCODE: 0x2BA01477.
Designer: 0x23B, Part Number: 0xBA01, Version: 0x2.
ID-Code read correctly at 1.00 MHz.
JTAG-SWD Debug Port enabled.
Scanning AP map to find all APs.
AP[0] IDR: 0x24770011, Type: AMBA AHB3 bus.
AP[0] ROM table base address 0xE00FF000.
CPUID: 0x412FC231.
Implementer Code: 0x41 - [ARM].
Found Cortex M3 revision r2p1.
Cortex M3 Core halted [0.001 s].
Device chip version:
 * Device official code is HVC4420.
 * Device version is B1.
 * Device CUST is 0xF (Flash).
 * Device ROM version 0x0 (Flash).
 * SWD Debug Interface is enabled.
 * Window Watchdog is not enabled.
 * Digital Watchdog is not enabled.
Requested Clock is 37.50 MHz.
Generated Clock is 37.50 MHz.
Good samples: 3 [Range 4-6].
IDCODE: 0x2BA01477.
Designer: 0x23B, Part Number: 0xBA01, Version: 0x2.
ID-Code read correctly at 37.50 MHz.
Time for Connect: 0.107 s.
>|
---#TPCMD MASSERASE F
Start Masserase operation.
Time for Masserase F: 0.043 s.
>|
---#TPCMD BLANKCHECK F
Start Blankcheck operation.
Time for Blankcheck F: 0.009 s.
>|
---#TPCMD PROGRAM F
Start Program operation.
Time for Program F: 2.730 s.
```


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```
>|
---#TPCMD VERIFY F R
Start Verify Readout operation.
Time for Verify Readout F: 0.032 s.
>|
---#TPCMD VERIFY F S
Start Verify Checksum 32bit operation.
Time for Verify Checksum 32bit F: 0.010 s.
>|
---#TPCMD DISCONNECT
>|
```

1 – TDK HVC 64KB example Programming Times

Operation	Timings FlashRunner 2.0
Time for Connect	0.107 s
Masserase Flash	0.043 s
Blankcheck Flash	0.009 s
Program Flash	2.730 s
Verify Readout Flash	0.032 s
Verify Checksum Flash	0.010 s
Cycle Time	**00:02.934 s**

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TDK HVC Driver Changelog

Info about driver version 5.00 - 30/04/2024
First official version for driver HVC.
Supported all TDK HVC4xx series.

Info about driver version 5.01 - 30/05/2024
Added new command `#TPCMD SET_READOUT_PROTECTION` to enable the HVC device Readout Protection.
Updated also Program command for NVRAM memory to manage Readout Protection activation.

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